

## REMARKS

Reconsideration and allowance of the present application are respectfully requested. By way of the above amendments, claims 1, 17, 19, 27 and 31 have been amended. Claims 1-31 currently are pending.

Independent claim 1 has been amended to recite that the means for arbitrating establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy. Independent claim 17 has been similarly amended with respect to a step of arbitrating. Support for these amendments is found throughout the original disclosure, for example, in original claim 19 and in the specification, paragraphs 0005, 0007, 0031, 0032, 0040, 0041, 0047, 0052, and 0055-0058. Subject matter added to claims 1 and 17 has been deleted from dependent claim 19. Remaining amendments made to claims 1, 17, 27 and 31 correct minor informalities and/or improve readability.

On page 2, Section 3 of the Action, claim 2 was objected to for allegedly not being definite with respect to which system bus recited in claim 1 forms a basis for its recitation of "said system bus." It is respectfully submitted that the amendment to independent claim 1 fully addresses the concerns expressed in Section 3 of the Office Action. As such, Applicants request the Examiner to withdraw the objection to claim 2.

The Office Action includes a rejection of claims 17-31 under 35 U.S.C. § 112, second paragraph, for allegedly being indefinite. This rejection is respectfully traversed. The Office Action alleges that the language "the flow of information" recited in claim 17, "the time required to transfer one data packet" recited in claim 27, and "said destination device" recited in claim 37, are indefinite. Applicants

respectfully submit, however, that one of ordinary skill in the art would have understood the meaning of these recitations, especially when they are read in the context of the remainder of the claim and in light of the specification. However, to improve readability and provide explicit basis for the recited features, claims 17, 27 and 31 have been changed. It is respectfully submitted that these changes render moot the rejection under Section 112.

In Section 7 of the Office Action, claims 1-7, 14-18 and 28 were rejected under 35 U.S.C. § 103 as being unpatentable over Kimura (Japanese publication no. JP 409022380 A) in view of Yamagami et al. (Japanese publication no. JP 408272756 A). This rejection is respectfully traversed.

The present invention is directed to bus systems for transferring information between multiple processors. Applicant's Figure 1 shows an exemplary apparatus for managing flow of information among plural processors of a processor array. The Figure 1 embodiment includes a number of processor modules 114, 116 and 118 which are connected by way of a system bus 102. In the Figure 1 embodiment, the system bus 102 also interconnects a system bus arbitration unit 112 for controlling access to the system bus by the various processors 114, 116 and 118 connected thereto. This access is arbitrated independently of the processors connected by the system bus 102. As shown in Applicant's Figure 2, exemplary system bus arbitration logic 202 and/or module bus arbitration logic 208 receives receiver busy bit (RBB) signals (e.g., see signals [.]RBB[.]\* of Figure 2) provided by each destination interface used by the arbitration logic and indicated when a device (e.g., one of the processors 114, 116, 118 and 124) is busy.

In accordance with the invention, clear (i.e., not busy) path segments are identified by way of RBB signals before any information is sent over the segment. Such a feature avoids attempts to transfer information over portions of the bus which are busy, or to processors which are unable to respond at that point in time to the information. In many conventional bus architecture systems, by contrast, it is necessary to incorporate wait states or transition aborts in cases where the system bus is too busy to transmit a message, or a receiving destination is incapable of receiving a transmission. However, the present invention eliminates the need for such wait states or transition aborts as the bus arbitration logic ensures that each destination is capable of receiving a packet before access to the system bus 102 is granted.

The foregoing features are broadly encompassed by Applicant's amended independent claim 1. Claim 1 is directed to an apparatus for managing flow of information among plural processors of a processing array. The apparatus comprises a system bus for interconnecting at least two processors and means for arbitrating access to at least a first portion of the system bus among said at least two processors to transfer information over said first portion. The claim 1 apparatus includes means for arbitrating which establishes a clear path to a device by checking device busy signals to ensure that a destination device is not busy. Claim 1 recites that the information is transferred using a protocol by which the system bus performs control actions for system bus access independently of said at least two processors. Such features are neither taught nor suggested by the Kimura and Yamagami et al. publications whether considered together, or in any combination with the PCI System Architecture publication (hereinafter, the PCI publication).

In the Office Action, the Examiner correctly acknowledges that Kimura and Yamagami et al. fail to teach or suggest arbitrating that comprises “establishing a clear path to a device by checking device busy signals to ensure that a destination device is not busy” (see, page 8, lines 21-23). Therefore, the Examiner, with reference to page 86, step 6, relies on the PCI publication for teaching device busy signals “TRDY#” and “IRDY#” that allegedly ensure that a destination device is not busy. It is respectfully submitted, however, that the Examiner’s interpretation of the PCI publication concerning these busy signals mischaracterizes what is taught in the relied upon parts of this document. The PCI publication discloses that the signal IRDY# is monitored by an arbiter to determine if the *bus* is busy before parking on the bus (see, page 83, the first scenario and Table 6-1). Step 6 of page 87 discloses that IRDY# is sampled to indicate that target data is *present on the bus*. It does not imply, teach or suggest that the signals TRDY# and IRDY# are checked *by an arbiter to ensure that a destination device is not busy* to establish a clear path to the destination device.

For at least these reasons, the proposed combination of references fail to teach or suggest each and every feature set forth in the independent claim 1 combination. Similar distinctions are recited in independent claim 17. For instance, claim 17 is directed to a method for managing flow of information among plural processors of a processing array that comprises, *inter alia*, a step of arbitrating access including establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy. For reasons similar to those given above, it is respectfully submitted that the Kimura, Yamagami et al., and

PCI publication documents fail to teach or suggest this feature in the context in which it is claimed.

It is respectfully submitted that the Sand et al. and MacDonald et al. patents likewise do not teach or suggest the claimed combinations set forth in independent claims 1 and 17 that include, among other features, establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy. Hence, no combination of the Kimura publication, the Yamagami et al. publication, the PCI publication, the Sand et al. patent and the McDonald et al. patent would have taught or suggested what is set forth in independent claims.

Because none of the documents relied upon by the Examiner teach or suggest significant features of the combinations of features set forth in independent claims 1 and 17, these independent claims are patentably distinct over these documents. As such, claims 1 and 17 are considered allowable.

The remaining claims 2-16 and 18-31 depend from one of independent claims 1 and 17 and recite further advantageous features which further distinguish over the documents relied upon by the Examiner. As such, these claims also are considered patentable.

In view of the foregoing, Applicant respectfully submits that the application is in condition for allowance. Prompt notification of the same is earnestly solicited so the issuance of the application will not be further delayed.

Respectfully submitted,

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Date: August 19, 2004

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